

10/635,363



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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:

Alin Theodor Iacob

Appln. No.: 10/635,363

Filed: August 6, 2003

For: WAFER, WAFER DICING SYSTEM,
AND METHOD OF DICING THE WAFER

Group Art Unit: 2826

Examiner: Tan N. Tran

RESPONSE TO RESTRICTION
REQUIREMENT AND PRELIMINARY
AMENDMENT

INTRODUCTORY COMMENTS

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This is a Response to a Restriction Requirement and a Preliminary Amendment. Please amend the above-identified application as follows:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper; and

Remarks which begin on page 8 of this paper;

Adjustment date: 10/13/2004 SDIRETA1
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Dated: July 1, 2004 By: [Signature]

RESPONSE TO RESTRICTION
REQUIREMENT AND PRELIMINARY AMENDMENT

Atty. Docket No. 100-22100
(P05626)

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Examiner: Tran, Tan N.

REQUEST FOR REFUND

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Director of the US Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Applicants' attorney received a monthly statement of Deposit Account dated July 30, 2004, indicating \$36 was debited from Account No. 502305 on July 26, 2004 for Fee Code 1202 regarding a Preliminary Amendment filed July 1, 2004 (copy enclosed). The Preliminary Amendment consists of claims 1-22 and 31-33, claims 23-30 being cancelled. There are currently 3 independent claims and 22 dependent claims, for a total of 25 total claims. The application filed on August 6, 2003, contained 3 independent claims and 28 dependent claims, for a total of 31 claims for which a check was submitted in the amount of \$988.00 of which \$198 was for the 11 extra total claims (copy enclosed). As a result, there is no additional fee to file the Preliminary Amendment. Accordingly, applicants' attorney respectfully requests a refund in the amount of \$36 to be credited to our Deposit Account No. 502305.

Respectfully submitted,

Dated: 9-8-04By: Mark C. Pickering

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Attorney for Assignee

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Atty. Dkt. No. 100-22100
(P05626)

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Application Number

10/636,363

Filing Date

August 6, 2003

First Named Inventor

Ali Theodor Jacob

Group Art Unit

2828

Examiner Name

Tuan Tan N.

Attorney/Agent Number

100-22100 (P06626)

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Mark C. Pickering, Reg. No. 36,236

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July 1, 2004

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July 1, 2004

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Group Art Unit: 2826

Examiner: Tan N. Tran

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REQUIREMENT AND PRELIMINARY
AMENDMENT****INTRODUCTORY COMMENTS**Commissioner for Patents
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Dated July 1, 2004 Mark C. Pi

**RESPONSE TO RESTRICTION
REQUIREMENT AND PRELIMINARY AMENDMENT**Atty. Docket No. 100-22100
(P05626)

10/635,363

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AMENDMENTS TO THE CLAIMS

1. (Original) A semiconductor wafer comprising:

a plurality of semiconductor circuits formed on the semiconductor wafer, each semiconductor circuit having a pair of first sides that are parallel to each other, and a pair of second sides that are parallel to each other and perpendicular to the pair of first sides;

a plurality of first saw streets that run parallel to the first sides between a number of the semiconductor circuits;

a plurality of second saw streets that run parallel to the second sides between a number of the semiconductor circuits;

a first metal trace formed between a first saw street and a first semiconductor circuit; and

a second metal trace formed between the first saw street and a second semiconductor circuit, the first saw street lying between the first semiconductor circuit and second semiconductor circuit.

2. (Original) The wafer of claim 1 wherein the first and second metal traces extend across the wafer.

3. (Original) The wafer of claim 1 wherein the first metal trace includes a first section and a second section that lie along side the first saw street, the second section having an extension section that extends away from the second section towards the first saw street.

4. (Original) The wafer of claim 3 wherein the second section has a plurality of extension sections that extend away from the second section towards the first saw street, each extension section having a first leg and a second leg that are

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REQUIREMENT AND PRELIMINARY AMENDMENT

Atty. Docket No. 100-22100
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connected together at a first end, and spaced apart and connected to the second section at a second end.

5. (Original) The wafer of claim 4 wherein the extension sections extend varying distances away from the second section towards the first saw street.

6. (Original) The wafer of claim 5 wherein an extension section extends into the first saw street.

7. (Original) The wafer of claim 4 and further comprising:
a reference element formed adjacent to the first and second sections;
a third metal trace that is connected to a first end of the resistive element;
and
a fourth metal trace that is connected to a second end of the resistive element.

8. (Original) The wafer of claim 7 wherein the reference element is a resistor.

9. (Original) The wafer of claim 3 and further comprising:
a third metal trace that lies between the first semiconductor circuit and the first saw street; and
an extending section that extends away from the second section towards the first saw street, the extending section contacting the first metal trace and the third metal trace.

10. (Original) The wafer of claim 9 wherein the extending section extends into the first saw street.

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REQUIREMENT AND PRELIMINARY AMENDMENT

Atty. Pocket No. 100-22100
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11. (Original) The wafer of claim 1 wherein:
the first metal trace runs parallel to the first saw street and then turns and runs parallel to a second saw street; and
the second metal trace runs parallel to the first saw street on an opposite side of the first saw street as the first metal trace, and then turns and runs parallel to the second saw street in an opposite direction as the first metal trace.

12. (Original) The wafer of claim 11 and further comprising:
a third metal trace that runs parallel to the first saw street and then turns and runs parallel to the second saw street on an opposite side of the second saw street as the first metal trace; and
a fourth metal trace that runs parallel to the first saw street and then turns and runs parallel to the second saw street in an opposite direction as the third metal trace on an opposite side of the second saw street as the second metal trace.

13. (Original) The wafer of claim 12 and further comprising:
a fifth metal trace that runs parallel to a third saw street and then turns and runs parallel to a fourth saw street;
a sixth metal trace that runs parallel to the fifth metal trace along an opposite side of the third saw street and then turns and runs parallel to the fourth saw street in an opposite direction as the fifth metal trace, terminating at the first metal trace; and
a seventh metal trace that runs parallel to portions of the fifth and sixth metal traces, terminating at the first metal trace.

14. (Original) The wafer of claim 1 wherein:
the first metal trace is formed around three sides and a portion of a fourth side of the first semiconductor circuit; and

RESPONSE TO RESTRICTION
REQUIREMENT AND PRELIMINARY AMENDMENT

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the second metal trace is formed around three sides and a portion of a fourth side of the second semiconductor circuit.

15. (Original) The wafer of claim 14 and further comprising a third metal trace formed around three sides and a portion of a fourth side of a third semiconductor circuit.

16. (Original) The wafer of claim 14 and further comprising a third metal trace formed around both the first semiconductor circuit and a third semiconductor circuit.

17. (Original) The wafer of claim 14 wherein the first and second metal traces are formed in a first level; and further comprising a third metal trace formed around three sides and a portion of a fourth side of the first semiconductor circuit, the third metal trace lying above and being spaced apart from the first metal trace.

18. (Original) A wafer dicing system comprising:
a resistance measuring system that measures the resistances of a plurality of metal traces formed on a wafer; and
a system controller connected to the resistance measuring system that controls the resistance measuring system and processes the resistance values measured by the resistance measuring system.

19. (Original) The wafer dicing system of claim 18 wherein the resistance measuring system includes:
a first multiplexer;
a second multiplexer; and
a resistance detector connected to the first and second multiplexers and the system controller.

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REQUIREMENT AND PRELIMINARY AMENDMENT

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20. (Original) The wafer dicing system of claim 19 and further comprising:
a cutting device; and
a cutting controller connected to the cutting device and the system controller.

21. (Original) The wafer dicing system of claim 18 wherein the resistance measuring system includes:
a plurality of resistance detectors; and
a multiplexer connected to the plurality of resistance detectors and the system controller.

22. (Original) The wafer dicing system of claim 21 and further comprising:
a cutting device; and
a cutting controller connected to the cutting device and the system controller.

Claims 23-30 (Cancelled)

31. (Original) The wafer dicing system of claim 18 wherein the system controller outputs a maintenance signal that indicates that maintenance is necessary.

32. (New) A semiconductor wafer comprising:
a plurality of semiconductor circuits formed on the semiconductor wafer, each semiconductor circuit having a pair of first sides that are parallel to each other, and a pair of second sides that are parallel to each other and perpendicular to the pair of first sides;

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a plurality of first saw streets that run parallel to the first sides between a number of the semiconductor circuits; and

a plurality of second saw streets that run parallel to the second sides between a number of the semiconductor circuits.

33. (New) The semiconductor wafer of claim 32 and further comprising a first metal trace formed between a first saw street and a first semiconductor circuit.

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REMARKS

This is a response to a restriction requirement and a preliminary amendment. The Examiner required that the invention be restricted to claims 1-22 and 31 which are drawn to a semiconductor device, or claims 23-30 which are drawn to a method of manufacturing a semiconductor device. As a result, applicant elects to prosecute claims 1-22 and 31 without traverse. In addition, by way of preliminary amendment, applicant has cancelled non-elected claims 23-30, and added claims 32-33 to additionally claim the present invention. As a result, claims 1-22 and 31-33 are currently pending.

Respectfully submitted,

Dated: 7-1-04By: Mark C. Pickering

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(P05626)

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8/6/2003

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Mark C. Pi

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